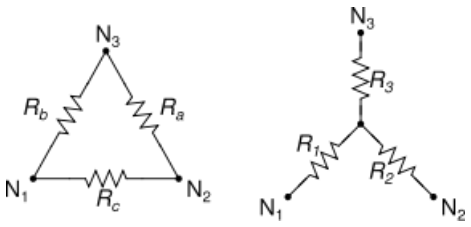
Work for Digital Electronics Supervision IV

Please attempt all the core items as usual and send your work to me by 1800 on Thursday, 5th November. All your answers, working and any additional thoughts should be written up in LaTeX and emailed to `mti20@cam.ac.uk`.

Core questions

1. Examples sheet exercises 19, 21, 22.

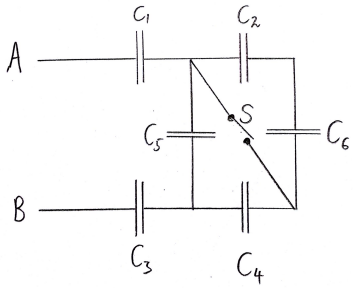
2. For what values of R_a, R_b and R_c is the resistor network on the left of the following diagram equivalent to the resistor network on the right?



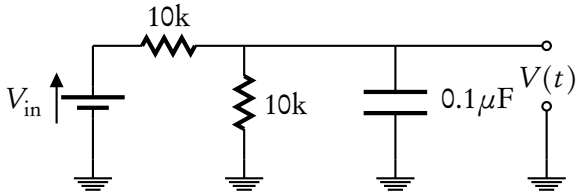
3. Derive the familiar equations describing resistors/capacitors in series/parallel:

$$R_{\text{series}} = \sum_i R_i \qquad \frac{1}{R_{||}} = \sum_i \frac{1}{R_i} \qquad \frac{1}{C_{\text{series}}} = \sum_i \frac{1}{C_i} \qquad C_{||} = \sum_i C_i$$

4. Find the capacitance across terminals A and B when the switch S is open, and when it is closed.



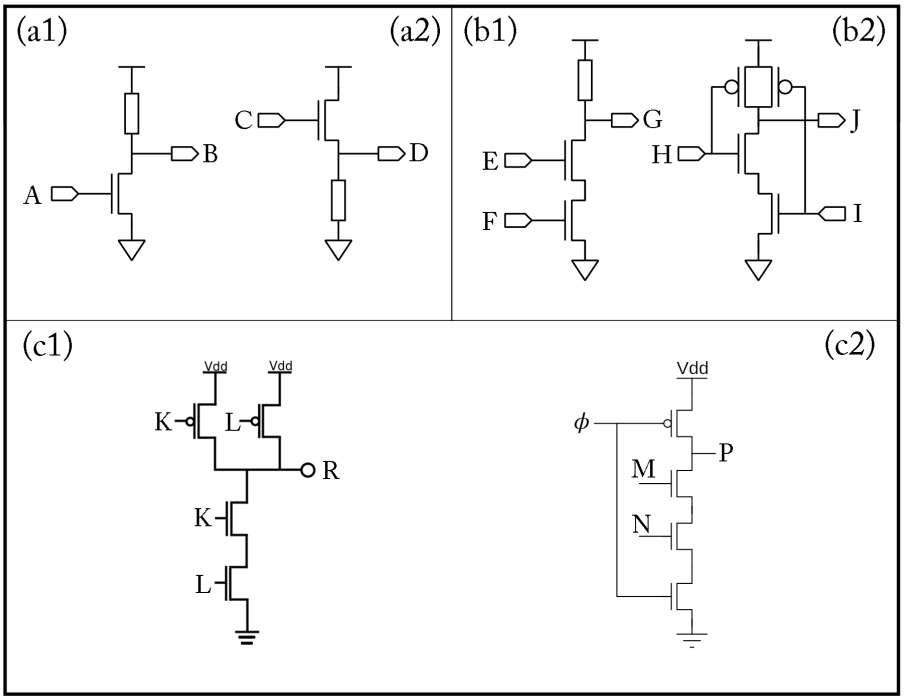
5. Find and sketch $V(t)$ in the following circuit:



6. (a) Give a qualitative explanation of current flow across a *p-n junction* in a semiconductor diode.
   (b) Why is there a depletion layer in the immediate vicinity of the junction?
   (c) Why is a resistor usually placed in series with a light-emitting diode? Given an LED which is to be driven from a 5V supply, what should be the value of the series resistor?

7. Examination question: 2012 Paper 2 Question 2 (attached towards the end of this document).

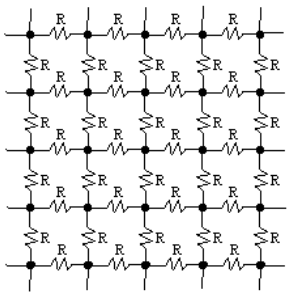
8. Three pairs of circuits (a1, a2), (b1, b2) and (c1, c2) are presented below. What is the operation of each individual circuit, and how does it compare with its pair?



9. (a) Sketch a transistor-level circuit for a 2-input AND gate in static CMOS.
   (b) Consider the design of a 16-input AND gate in static CMOS.
      i. Explain why the 2-input design could not simply be scaled up.
      ii. Sketch alternative designs using two and four levels of NAND and NOR gates.

Extension questions

10. Consider an infinite grid of resistors connecting adjacent nodes of a square lattice:



Between every pair of adjacent nodes is a resistance R. The grid extends to infinity in all directions. Determine the effective resistance between any two adjacent nodes in the lattice.

11. The tiles in the floor of the "street" (public walk way) in the William Gates Building show the pattern of a punched paper tape along its length. Decode the message.

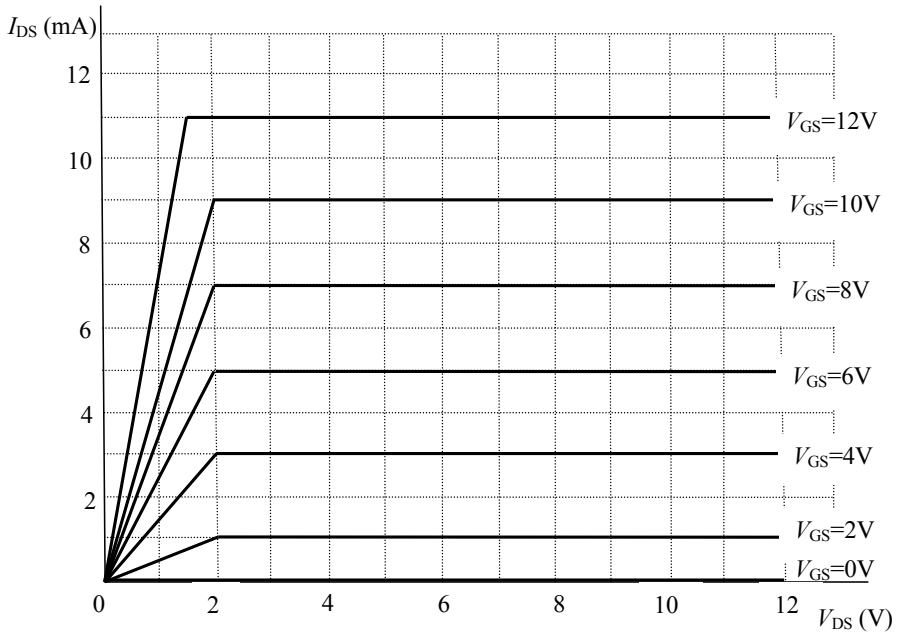
COMPUTER SCIENCE TRIPOS Part IA – 2012 – Paper 2

2 Digital Electronics (IJW)

(*a*) With the aid of appropriate diagrams, show how the Source–Drain current that flows in a p-channel MOSFET is controlled by the applied Gate–Source voltage. [4 marks]

(*b*) (*i*) Draw the circuit diagram of a NOT gate that comprises an n-channel MOSFET and a resistor R. [2 marks]

(*ii*) For the NOT gate in (*b*)(*i*), plot the relationship between the input voltage, V_{in} and the output voltage, V_{out}. Assume that the power supply voltage $V_{\text{DD}} = 12$ V, $R = 1$ kΩ, and that the MOSFET has the characteristics given in the following figure. [4 marks]



(*c*) For the NOT gate in (*b*), calculate the power dissipated by the entire gate and that by resistor R alone, when $V_{\text{in}} = 12$ V. [4 marks]

(*d*) The stray capacitance present at the output of the NOT gate in (*b*) can be represented by a capacitor, $C = 100$ nF connected between the gate output and 0 V. Also assume that the MOSFET has an ON resistance $R_{\text{on}} = 100$ Ω. The input signal, V_{in}, is a 1 kHz square wave with minimum and maximum amplitudes of 0 V and 12 V respectively.

(*i*) Sketch the output signal waveform, V_{out}, of the NOT gate being sure to include indicative rise and fall times and voltage levels. [4 marks]

(*ii*) How could the rise-time of V_{out} be reduced and what would be the impact of your proposed solution on the power dissipation of the circuit?